

JUL 05 2006

1374.39812VV2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: K. YAMAZAKI, et al.  
Serial No.: 10/639,465  
Filed: AUGUST 13, 2003  
Title: FABRICATION METHOD FOR SEMICONDUCTOR  
INTEGRATED CIRCUIT DEVICE  
Group AU: 1763  
Examiner: George A. Goudreau  
Confirm. No.: 6745

**TERMINAL DISCLAIMER**

**Mail Stop: AMEND - FEE**

Commissioner for Patents  
P. O. Box 1450  
Alexandria, VA 22313-1450

July 5, 2006

Sir:

Petitioner, Renesas Technology Corp., having its place of business at 4-1, Marunouchi 2-chome, Chiyoda-ku, Tokyo, Japan, represents that it is the sole owner of the entire interest of U.S. Application No. 10/639,465, filed August 13, 2003, for FABRICATION METHOD FOR SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE, and that the Assignment of all rights in connection therewith has been recorded at Reel 015472, Frame 0479.

Petitioner hereby disclaims all that portion of the term of any patent to be issued on the above-identified application subsequent to the expiration date of the full statutory term, defined in 35 USC 154 to 156 and 173, of U.S. Patent No. 6,479,392, issued November 12, 2002, and hereby agrees that any patent issued on the above-identified application shall be enforceable only for and during such time as said U.S. Patent No. 6,479,392 and the above-identified application are commonly owned.

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Docket No. 1374.39812VV2  
Appln. No. 10/639,465  
July 5, 2006

Petitioner, however, does not disclaim the terminal part of any patent granted on the instant application prior to the expiration date of the full statutory term, defined in 35 USC 154 to 156 and 173, of the above-listed U.S. Patent No. 6,479,392, in the event that U.S. Patent No. 6,479,392 expires: for failure to pay a maintenance fee; is held unenforceable; is found invalid; is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321; has all claims cancelled by a reexamination certificate; is reissued; or is otherwise terminated prior to expiration of the above-referred-to full statutory term, except for the separation of legal title as stated above.

This disclaimer is to be binding with respect to any patent granted on the above-identified application, and is binding upon grantees, their successors, or assignees of any interests.


The undersigned is an attorney of record in this application and is empowered to act on behalf of Renesas Technology Corp. for execution and submission of Terminal Disclaimers, in accordance with the provisions of 37 CFR 1.321(b) and (c), effective January 4, 1994.

Docket No. 1374.39812VV2  
Appln. No. 10/639,465  
July 5, 2006

The undersigned hereby declares that all statements made herein of his knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine, or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Respectfully submitted,

**ANTONELLI, TERRY, STOUT & KRAUS, LLP**

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